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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/912,745	07/24/2001	Richard A. Zatorski	2070.001700	5356

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EXAMINER	
LEFKOWITZ, SUMATI	

ART UNIT	PAPER NUMBER
2112	

DATE MAILED: 09/27/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/912,745	ZATORSKI, RICHARD A.	
	Examiner	Art Unit	
	Sumati Lefkowitz	2112	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 July 2004 and 02 August 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *02 August 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-18 are pending.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1,4-9, and 12-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Blackledge, Jr. et al., 5,835,738 (hereinafter Blackledge) in view of Applicant's Admitted Prior Art (hereinafter AAPA).

As to claims 1, 4-9, and 12-17, Blackledge discloses a bus bridge circuit (note Figure 2, bridge 50), wherein the bus bridge circuit is adapted for coupling to a first bus (note Figure 2, bus 58) comprising n address lines, and wherein n is an integer and n>=2 (i.e., inherent to microchannel bus), and wherein the bus bridge circuit comprises; and an addressable register (note Figure 3, bridge translation register 62) comprising a bit position for storing an additional address bit; the bus bridge circuit configured drive an n-bit address upon the n address lines of the first bus (note column 5, line 22 – column 6, line 44, column 11, line 51 – column 12, line 40), 4: that the first bus is a peripheral component interconnect (PCI) bus having n multiplexed address/data lines (note column 5, lines 33-39), 5: that the bus bridge circuit is further adapted for coupling to a second bus, and wherein the bus bridge circuit is configured to translate signals

between the first bus and the second bus (note column 5, lines 22-39), 6: that the first bus is a peripheral component interconnect (PCI) bus having n multiplexed address/data lines, and wherein the second bus is an industry standard architecture (ISA) bus (note column 6, lines 7-16).

Although Blackledge fails to disclose that the bus bridge circuit is configured to: concatenate the additional address bit with an n-1 bit address to produce the n-bit address, wherein the additional address bit forms a most significant bit of the n-bit address, Blackledge does disclose that the bus bridge circuit is configured to concatenate additional address bits stored in a register with an input address, not of length n-1 bits, to produce an n-bit address, wherein the additional address bits form most significant bits of the n-bit address (note column 5, line 22 – column 6, line 44, column 11, line 51 – column 12, line 40).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to employ the use of any number of additional address bits, including 1, required to translate an input address, including one with n-1 bits, to an address which is compatible with the bus over which the address is to be transmitted, since the actual number of bits to be concatenated/added would not alter the underlying function of concatenating most significant bit(s) to an address to make the address compatible with the bus over which the address is to be transmitted.

Blackledge also fails to disclose that the bus bridge circuit comprises audio logic configured to access digital audio data and to produce an n-1 bit address when accessing the digital audio data or that address translation takes place when the audio logic accesses the digital audio data.

AAPA discloses that the bus bridge circuit comprises audio logic configured to access digital audio data and to produce an n-1 bit address when accessing the digital audio data and that address translation from n-1 to n bits takes place when the audio logic accesses the digital audio data (note [0008-0009]), 7: wherein the audio logic is adapted for coupling to a speaker, and wherein the audio logic is configured to receive digital audio data, to transform the digital audio data to an analog signal, and to provide the analog signal to the speaker (note [0008]), 8: wherein the audio logic is adapted for coupling to a microphone, and wherein the audio logic is configured to receive an analog signal from the microphone, to transform the analog signal to digital audio data representing the analog signal, and to provide the digital audio data (note [0008]).

It would have been obvious to one of ordinary skill in the art at the time of the invention to employ the use of audio logic in the bridge of Blackledge, as AAPA teaches, so as to allow the bridge to be coupled to a speaker an/or an audio source, as AAPA teaches in [0008] and also to allow mass production of the bridge chip including audio logic, due to the integration of the audio logic within the bridge chip.

4. Claims 2 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Blackledge, Jr. et al., 5,835,738 (hereinafter Blackledge) in view of Applicant's Admitted Prior Art (hereinafter AAPA), as applied to claims 1 ,4-9, and 12-17 above, and further in view of Jander et al., 5,857,080 (hereinafter Jander).

As to claims 2 and 10, Blackledge fails to disclose that the addressable register has an

address and wherein a value may be stored in the addressable register via a write operation specifying the address of the addressable register.

Jander discloses that an addressable register has an address and a value may be stored in the addressable register via a write operation specifying the address of the addressable register (note column 5, lines 8-41 and column 6, lines 32-45).

It would have been obvious to one of ordinary skill in the art at the time of the invention to employ the use of an addressable register for storing a value via a write operation specifying the address of the addressable register, as Jander teaches, in the system of Blackledge so as to allow more flexibility in the placement of information at locations most convenient for developing the translations necessary for transferring information, as Jander teaches in column 4, line 65 – column 5, line 4.

5. Claims 3, 11, and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Blackledge, Jr. et al., 5,835,738 (hereinafter Blackledge) in view of Applicant's Admitted Prior Art (hereinafter AAPA), as applied to claims 1 ,4-9, and 12-17 above, and further in view of Jander et al., 5,857,080 (hereinafter Jander) and what was well known in the art as exemplified by Henning et al., 5,835,430 (hereinafter Henning).

As to claim 3, 11, and 18, Blackledge discloses that the n address lines of the first bus define an address space of the first bus (i.e., inherent to any bus) but fails to disclose that a bit stored in the bit position of the addressable register via a write operation determines whether the n-bit address resides in a lower portion of the address space of the first bus, or in an upper portion of the address space of the first bus.

Jander discloses that an addressable register has a bit stored in the bit position of the addressable register via a write operation for specifying the location of an n-bit address in an address space (note column 5, lines 8-41 and column 6, lines 32-45).

It would have been obvious to one of ordinary skill in the art at the time of the invention to employ the use of an addressable register for storing a bit via a write operation for specifying the location of an n-bit address in an address space, as Jander teaches, in the system of Blackledge so as to allow more flexibility in the placement of information at locations most convenient for developing the translations necessary for transferring information, as Jander teaches in column 4, line 65 – column 5, line 4.

Examiner takes Official Notice that dividing or partitioning address spaces into any number of desired banks or segments and accessing the banks using a corresponding number of most significant bits of an address (for example, 1 bit would be used to select up to 2 banks, 2 bits up to 4 banks, 3 bits up to 8 banks, and so on) is well known in the art of addressing for the purpose of assigning dedicated addresses within address spaces to various devices, thereby establishing boundaries for devices and processes to work in without corrupting address spaces of other devices and processes, evidence of which may be found in Henning at column 3, lines 12-37.

It would have been obvious to one of ordinary skill in the art at the time of the invention to employ the use of any number of bits, including one, of the most significant bit of an address to specify one of any number of portions, including two, of address spaces in which to perform an access, since the number of bits employed would not alter the function of dividing the address space into various portions for association with various devices or processes.

Response to Arguments

Applicant's arguments filed 7/19/04 have been fully considered but they are not persuasive for the following reasons:

Blackledge is completely silent with respect to a bus bridge circuit comprising audio logic, as presented in claim 1. Therefore, Blackledge cannot possibly teach or suggest the bus bridge circuit of claim 1.

Blackledge was not used to teach a bus bridge circuit comprising audio logic. AAPA was used to teach a bus bridge circuit comprising audio logic.

AAPA teaches away from an addressable register comprising a bit position for storing an additional address bit.

AAPA was not used to teach an addressable register comprising a bit position for storing an additional address bit. Blackledge was used to teach an addressable register comprising a bit position for storing an additional address bit.

Jander is completely silent with respect to a bus bridge circuit comprising audio logic, as presented in claims 2 and 10. Therefore, Jander cannot possibly teach or suggest the bus bridge circuit of claims 2 and 10.

Jander was not used to teach a bus bridge circuit comprising audio logic. AAPA was used to teach a bus bridge circuit comprising audio logic.

Henning is completely silent with respect to a bus bridge circuit comprising audio logic, as presented in claims 3, 11, and 18. Therefore, Henning cannot possibly teach or suggest the bus bridge circuit of claims 3, 11, and 18.

Henning was not used to teach a bus bridge circuit comprising audio logic. AAPA was used to teach a bus bridge circuit comprising audio logic.

Conclusion

6. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Sumati Lefkowitz whose telephone number is 703-308-7790. The examiner can normally be reached on Monday-Friday from 6:00-2:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark Rinehart can be reached at 703-305-48154815.

The fax phone numbers for the organization where this application or proceeding is assigned are:

703-872-9306 for Official communications

703-746-5661 for Non-Official/Draft communications

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-3900.

Sumati Lefkowitz
Primary Examiner
Art Unit 2112

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September 23, 2004